

CAPACITOR BASICS III – Mechanical Configurations

Single Layer Vs Multilayer Designs

In their simplest form ceramic capacitors are comprised of a single sheet or layer of dielectric with electrodes printed on each side. This approach may be ideal for higher voltage, lower capacitance designs, but may not be considered practical for applications where a significant amount of capacitance is required. Material and process constraints place finite limitations on the overall maximum size of a plate and the minimum thickness that one can reliably cast dielectric. Once those limitations have been reached the engineer is forced to look at alternative methods by which these challenges can be managed and multilayer capacitor designs provide that option.

The most obvious difference in construction between a single layer and a multilayer capacitor is that the electrodes are external to the device for a single layer, whereas electrodes are basically encased in ceramic for the multilayer approach. Multilayer capacitors represent a design methodology whereby several alternating layers of ceramic and electrode material are stacked, pressed and fired together to form a single monolithic structure. In this configuration the dielectric thickness of each layer remains the same and the effective plate area is increased by virtue of having several individual capacitors connected in parallel.

Capacitor Basics I established that the capacitance value for a single layer device is defined by the following formula:

$$C = f \cdot \frac{K \cdot A}{t}$$

Where C = Capacitance (picofarads)
f = Conversion factor (0.2246 for English system of units or 0.0884 for Metric units)
K = Dielectric Constant for material used
A = Area of electrode that overlaps adjacent electrode (inch² or centimeter²)
t = Thickness of dielectric (inch or centimeter)

Using the above formula and an assumed dielectric thickness of 0.020", the required area needed to achieve 1.0 μF of capacitance using a ceramic material with a dielectric constant of 1500 would be as follows:

$$\begin{aligned} 1,000,000 \text{ pF} &= (0.2246 \times 1500 \times A) / 0.020 \\ A &= (1,000,000 \times 0.020) / (0.2246 \times 1500) \\ A &= 59.4 \text{ in}^2 \end{aligned}$$

If this were a single layer design, there are several potential issues to consider, not the least of which is a design that could conceivably be 8.5" long x 7" wide in one extreme, to as much as 59" long x 1" wide in the other. Assuming that a manufacturer in fact has the technology to produce such a design, the 0.020" thickness would leave this design extremely fragile. Of course beefing up the dielectric thickness to make the design more robust would be an option, but increases in dielectric thickness are inversely proportional to the capacitance value thereby requiring that the length and / or width be increased to compensate and maintain the required capacitance value.

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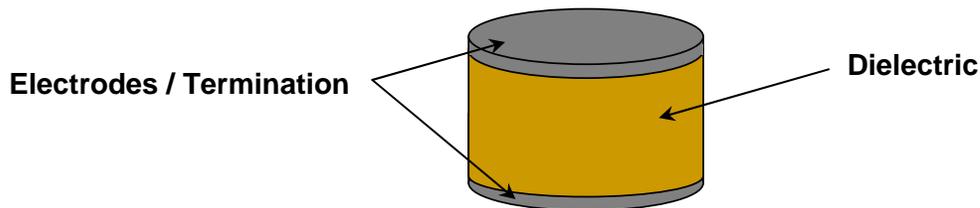
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If we were now to consider the option of manufacturing this capacitor as a multilayer, 10 layer design, the required area would remain the same, but now we are looking at a much more manufacturable design that is roughly 0.850" long by 0.700" wide by 0.200" thick. Not only is the length and width much more manageable, but at 0.200" thick plus cover sheets, the design would be much more robust.

Physical Options

Ceramic capacitors can be manufactured in a variety of shapes and sizes depending on the application. These configurations all incorporate the basic principle of multiple electrodes, separated by a dielectric material, set to a specific thickness to meet basic operational constraints such as capacitance value, working voltage and in some instances voltage coefficient. The following information provides basic fundamental information related to some of the more common design options.

- ⚙️ **Single Layer Discs** – The most basic approach to capacitor design would be the single layer disc. This design utilizes a dielectric layer that is generally formed thru a pressing process, although extrusion and casting of dielectric material can also be utilized. Once the dielectric has been fired a termination material, which acts as the electrodes, is applied to the top and bottom of the disc. Depending on the type of electrode material used, these discs can be soldered, welded or connected with conductive epoxy directly to a surface, or some type of metal lead can be attached to the termination for subsequent assembly into a circuit. A basic disc design is shown below:



Given the ability of this process to manufacture thick dielectric layers, these parts are commonly used in extremely high voltage applications, some as high as 50kVdc.

- ⚙️ **Multilayer Ceramic Chip Capacitors (MLCC)** – As indicated in section 1 of this chapter, multilayer ceramic capacitors allow the engineer to achieve much higher levels of capacitance in a much more robust design than would be available for a single layer device. In addition, with electrodes accessed thru end terminations, MLCC configuration are tailored towards board level surface mount designs which reducing handling and generally improves overall productivity.

The most common approach for manufacturing MLCC capacitors was described in Section II as a method whereby sheets of dielectric material are cast and dried, electrodes are printed, sheets are stacked, assemblies are baked out and fired and the monolithic device is terminated. The two generally accepted processes for casting material involve either a "wet" stack process or a "dry" stack process. Initially, both processes require that ceramic material be cast and dried into the "green" state and an electrode is printed on the surface. At this point, the "wet" process differs from the "dry" stack process inasmuch as the liquid slurry is cast over the previously printed green sheet whereas the dry process stacks individual printed green sheets. **Add additional info on benefits of wet vs dry**

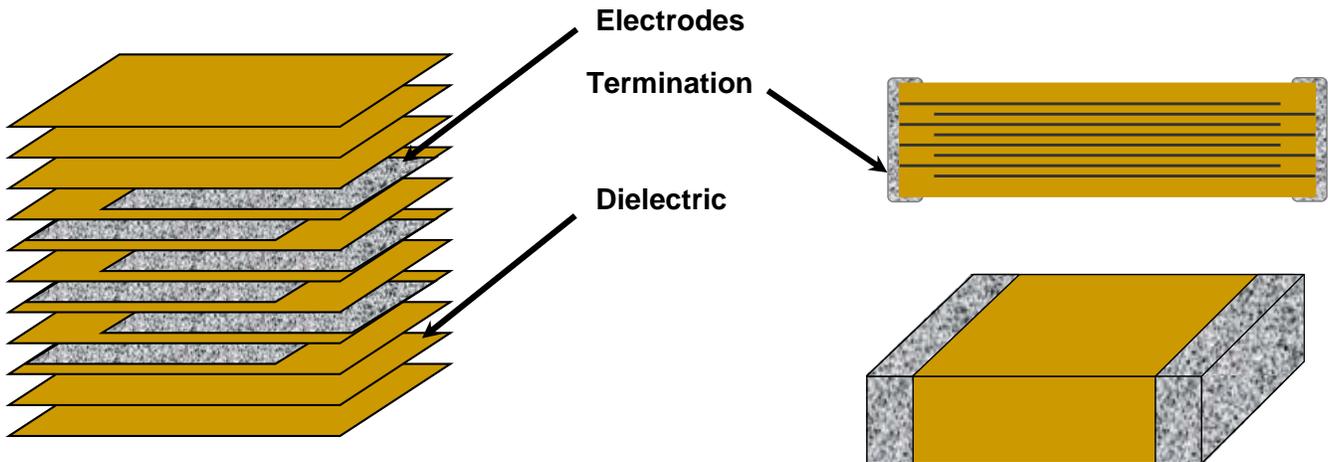


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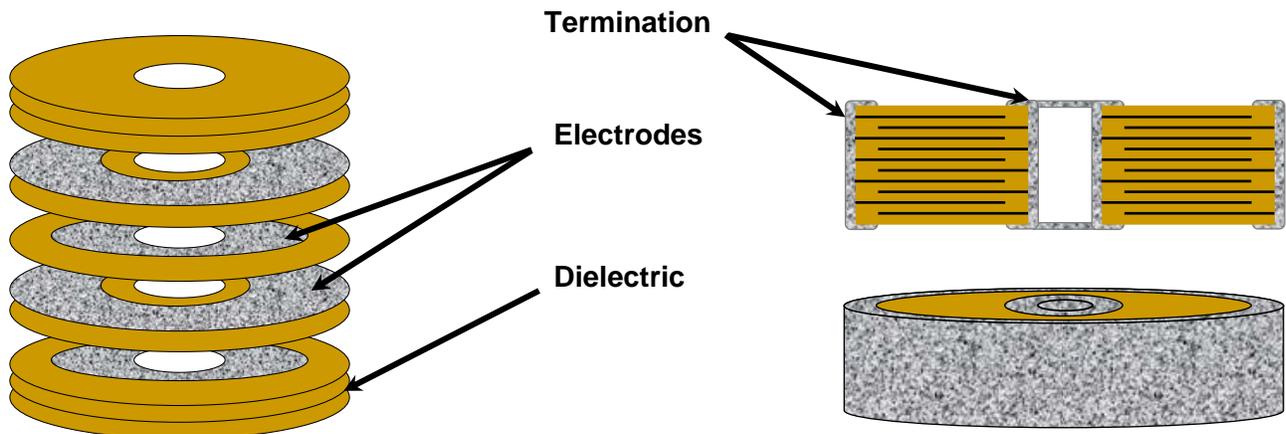
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Examples of an exploded layout, a cross – section and an outline drawing for an MLCC capacitor are shown below.



⚙️ **Discoidal Capacitors** – Discoidal capacitors provide another approach to the multilayer capacitor concept whereby alternating layers of ceramic and electrode material are stacked to achieve higher levels of capacitance in a robust monolithic structure. Unlike a typical MLCC, which makes electrode contact at opposite ends of the chip capacitor, the discoidal capacitor is donut shaped and opposing electrodes are connected by means of the inside and outside diameter. The physical characteristics of this approach provide for a complete 360° contact and extremely low levels of ESR and ESL. **Add info on specific applications, filter assemblies, etc**



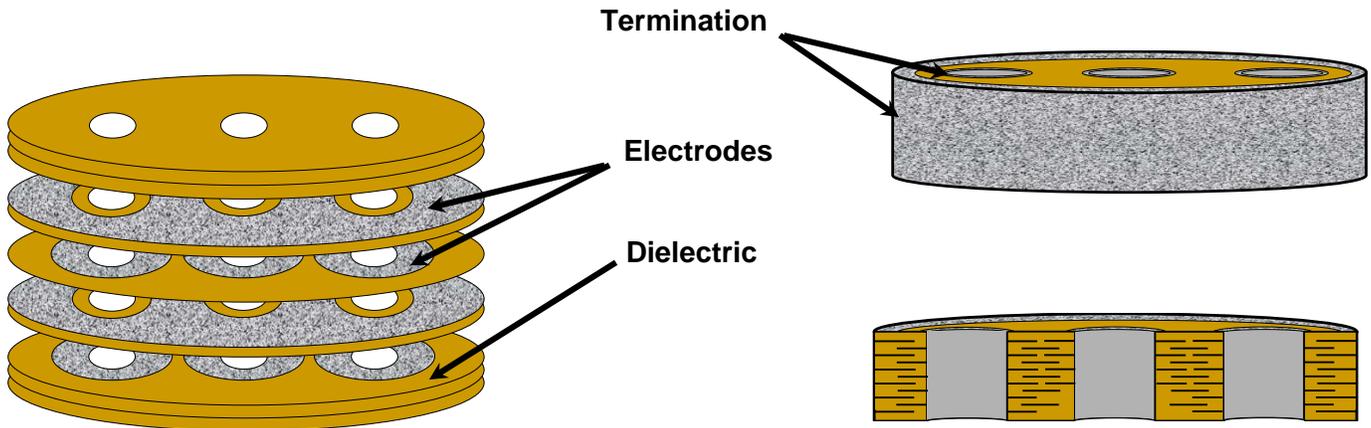
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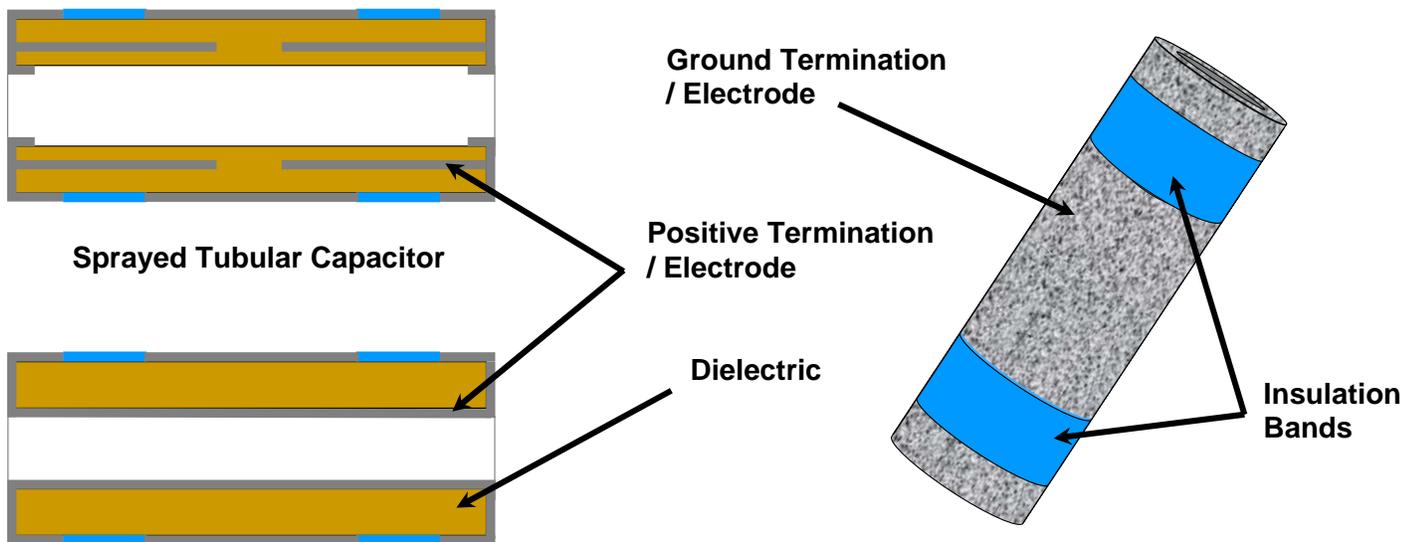
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- ✦ **Planar Arrays** - Expanded concept of discoidal technology.....Add basic info on design, benefits, issues flexibility of planar concept and mounting approaches.



- ✦ **Tubular Capacitors** – Tubular capacitors generally offer inexpensive, low capacitance value designs that are typically intended for EMI / RFI filtering applications. These capacitors are most often extruded or pressed, but can also be manufactured using a process that sprays dielectric onto a spindle, building it up gradually until a desired thickness is met. This manufacturing approach may be more costly than the other tubular options, but it does allow the engineer to incorporate a buried electrode and a much higher capacitance per unit volume. **Add info concerns and mounting approach...**



Pressed / Extruded Tubular Capacitor

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